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Dual Active Compensation for Voltage Source Rectifiers Under Very Weak Grid Conditions

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ABSTRACT DC subgrids consisting of modern active loads (ALs) and local dc distributed generation (DG) units are normally interfaced with the main ac grid by utilizing bidirectional voltage source converters (VSCs). Under the very weak grid (VWG) conditions, the integration of voltage-oriented controlled (VOC) VSCs in the inversion mode becomes very challenging and therefore undamped oscillations in the power and angle responses are yielded. Most of the existing works address this issue for VSCs in the inversion mode of operation. However, integration of VSCs in the rectification mode with the consideration of the outer loop controllers into the VWGs has not been reported. To fill up this gap, a state-space model of the bidirectional VSC-to-weak grid (VSC-WG) system is developed in this work with an emphasis on the rectification mode of operation. A modal-sensitivity analysis is then utilized to evaluate small-signal stability of the system, identify the dominant modes, and investigate the system states that have a major influence on these modes. The results reveal two pairs of unstable complex modes that are correlated with the dynamic interaction between the VOC-based VSCs and the VWG impedance. It is also shown that the stability margin of VSCs in the rectification mode is less than that of the inversion mode under the same VWG conditions. To enhance the integration of the VSCs in the rectification mode, a dual-active compensation (DAC) scheme is proposed to mitigate the instabilities under VWG conditions. Several time-domain simulation results are presented to verify the validity of the small-signal model and demonstrate the effectiveness of the DAC scheme under the VWG conditions. Finally, hardware-in-the-loop (HIL) real-time experimental results are presented to validate the simulation results.

INDEX TERMS Dual active compensation (DAC), dynamic interaction, rectification mode, short circuit ratio (SCR), small-signal stability, voltage source converter (VSC), very weak grid (VWG).

I. INTRODUCTION

Power electronic converters (PECs) are used to interface many types of clean and renewable resources of energy such as photovoltaic panels and fuel-cells to the ac power grid registering them as distributed generations (DGs) [1]. There are many types of loads such as battery banks, data centers, LEDs, induction motors drives, and plug-in electric vehicles all over ac grids that are connected to the grid via PECs. Moreover, PECs can operate as bidirectional interfaces between the main ac grid and dc subgrids, such as high-voltage dc (HVDC) or dc microgrid (dc MG) systems, managing the power flow between the two sides.

One of the most commonly used PECs in DG applications is the voltage source converter (VSC) [2]–[5] and, among them, the two-level VSC structure is the dominant block in medium and high-power applications [5]. A widely accepted control strategy in the industry for VSCs is the voltage-oriented control (VOC) method [6] (or current-mode control [5]). In the VOC method, the inner current control loops (CC) with fast dynamics, and outer control loops, including dc voltage control (DVC), ac voltage control (AVC), and phase-locked loop (PLL), with slower dynamics, are established in the direct-quadrature (*dq*) reference frame (*dq*-RF) which is synchronous with the grid voltage vector at

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the point of common coupling (PCC). If the VSC is connected to a stiff grid (SG), where the grid equivalent impedance is negligible, the variation in the PCC voltage magnitude and frequency can be neglected. Hence, the VSC output currents in the *dq* channels are proportional to the instantaneous active and reactive power exchanged between the VSC and the grid, respectively. Therefore, the design of the VOC becomes independent of the rest of the grid.

In certain cases, such as rural areas, islands, and charging stations for electric vehicles, the loads might be far away from the PCC [7]. Similarly, DG systems such as photovoltaic units and wind farms are usually located in distant places with respect to the center of loads [8]–[11]. Moreover, VSC-based HVDC systems and DC MG can be connected to high-impedance ac grids [12]–[14]. All these examples show that there can be long distances between the interfacing VSCs and the main ac grids. Therefore, the grid equivalent series impedance cannot be ignored. In these cases, the grid is known as a weak grid (WG) and the stability of the VSC-to-WG system (VSC-WG) becomes very challenging. The voltage at the PCC in WGs features large fluctuations especially during transients because the PCC voltage is a function of the VSC output current and power. In other words, the VOC-based VSC and the grid dynamics are undesirably coupled [15]. Therefore, the design of the VSC control system cannot be achieved without considering the main ac grid parameters. Moreover, the WG impedance might have a wide range of variations due to the loads variations, grid reconfigurations, and faults [7], [9], [16], [17]. However, to realize the plug-and-play characteristics in modern power systems [7], the control design needs to allow seamless integration of the VSC with no prior knowledge of the grid parameters.

The strength of a power grid against the connected VSC is usually evaluated by the *short circuit ratio,* which is the ratio of the ac grid symmetrical short circuit level at the PCC to the VSC rated dc power [18]. The ac grid is considered weak when $2 < SCR < 3$ (WG); and very weak (VWG), when $1 < SCR < 2$ [18]–[20]. If $SCR > 3$, the grid is regarded as a stiff grid (SG). The VOC of VSC has a detrimental effect on the stability of the grid-VSC interconnection and can shift the location of the system eigenvalues which might result in poorly damped dynamics and power oscillations [21]. The smaller the *SCR* level is, the more prone is the system to instability [22].

The interaction dynamics between the three-phase VSCs in the rectification mode and SGs are studied in [23]. Therein, the rectifier is initially modeled by an ideal constant power load (CPL) and it is shown that the CPL introduces a negative incremental resistance that becomes prominent at a certain level of power which excites the resonance frequency of the VSC *LC* filter and as a result, the system becomes unstable. Further investigation of this problem is carried out in [5]. According to [5], the resulting transfer function of the VSC represents a nonminimum-phase zero in the rectification mode which reduces the closed-loop stability margin of the grid-connected VSC whereas the system remains stable in the inversion mode.

Several studies about the VSC-WG systems have shown unstable interaction dynamics. According to [21], even without considering the outer control loops, i.e., the DVC, the AVC, and the PLL, instability can happen due to the interaction of the CC with the VWG impedance. In [1], [8], [17], [15], [24]–[30], it is shown that the interaction between the PLL unit of VSCs and the WG impedances can be another source of instability. This undesired phenomenon is called the grid synchronization instability (GSI) [1], [30]. This issue is also another limiting factor for the active power transfer between the WGs and VSCs [1]. Moreover, the instability due to the GSI is dependent on the operation mode of the VSC, such that the VSC-WG system is stable for a wider range of *SCR* in the inversion mode than in the rectification mode. In other words, a higher power transfer is allowed between the VSC and the WG when the VSC is operating in the inversion mode. Therefore, improving the system stability in the rectification mode is more critical than the inversion mode under VWG conditions; a challenge that has not been widely investigated in the literature.

Since a high-bandwidth PLL decreases the damping of the grid-connected VSC systems [1], [21], [30], several researchers have suggested the idea of reducing the PLL bandwidth as a remedy for fixing the GSI problem and increasing the real power transfer in VSC-WG systems. However, this method often results in a PLL with a very slow dynamic response which is not desirable (see e.g., [5], [31], [32]). Modifying the structure of the outer control loops, the AVC and PLL, by adding linear functions of output voltage and currents has been proposed to improve the VSC-WG stability [15], [26], [31], [33]. Essentially, these methods change the output impedance of the VSC such that the source-load admittance matching holds between the VSC and WG. Thus, the VSC-WG systems stability is preserved according to the Nyquist stability criterion [34]. However, most of these methods address the inversion mode of operation whereas the more challenging rectification mode is not considered. Further, the level of improvement in the VSC-WG system stability is limited to $SCR = 2$. The compensation of the VWG impedance with a negative virtual impedance that is injected by a front-end VSC has been achieved in an HVDC system assuming that the dc-side voltage is maintained sufficiently high and hence the overmodulation is avoided [32]. Moreover, the dc-side voltage is assumed to be a constant value, and therefore, the DVC is not applied to the VSC. The gain scheduling method is used to design the proposed outer AVC of a front-end VSC of an HVDC system [20]. Similar to [32], the VSC-WG system stability is maintained at $SCR = 1$ in both directions, yet, at the expense of a complicated AVC system that relies on a lookup table to evaluate four pairs of control parameters sets. However, the key disadvantage of the preceding methods is that the steady-state responses of the VSC are affected especially under the VWG conditions.

Emulating the characteristics of synchronous machines (SM) has inspired several researchers to develop power synchronization control (PSC) [19], [24], [36]. As a major feature of the PSC, the PLL loop is not required, and the inner CC is replaced by a voltage control loop. Therefore, the integration of VSCs into the VWG can be achieved. While the majority of works about PSC have been done for VSCs in the inversion mode, the rectification mode of operation is also suggested to improve the stability of the WGs when supplying several VSC-interfaced loads [22]. However, since the current is not directly controlled, the control system must dynamically switch to a current limiting operation under severe transients such as faults which is practically challenging [32]. Therefore, as long as stability issues in the VSC-WG systems can be mitigated, the VOC is still the preferred method [32].

A simple and effective method that can mitigate instabilities due to the interconnection of VOC-based VSCs, in the rectification mode, and ac grids, with extremely low *SCR*s, has not been presented in the literature so far. Motivated by this drawback, a simple and lossless dual active compensation (DAC) scheme is proposed in this work that can be effortlessly integrated into the existing VOC. Upon incorporating the proposed dual-compensation scheme, the dynamic responses of the VOC loops are not negatively affected, and the steady-state values remain unchanged. Therefore, there is no need to redesign the VSC control system. The contributions out of this work are enlisted as follows.

- Stability analysis and assessment of the operation of the VSCs in the inversion and rectification modes under the VWG condition.
- Development of an actively compensated VSC-WG system, using the proposed DAC compensator, to achieve stable performance in the rectification mode under the VWG condition.
- Development of the small-signal model of the VSC-WG system where the dynamics of VSC outer control loops and the proposed DAC are considered.
- Verification of the effectiveness of the compensated VSC-WG systems following large-signal disturbances such as step changes in the current and voltage references and grid angle disturbances.

The rest of the paper is structured as follows. In Section II, the nonlinear model of the VSC-WG system is developed in the *dq*-RF followed by a discussion about the VSC controller design. Section III discusses the correlation between the power transfer capability of VSC-WG system and the *SCR* in the rectification mode. In Section IV, a small-signal stability analysis of the VSC-WG system in the rectification mode is studied using the linearized model of the system. Then, the modal and sensitivity analyses are carried out under the VWG conditions. In Section V, the proposed DAC scheme is introduced which is followed by a discussion about designing the DAC parameters using the root-locus method.

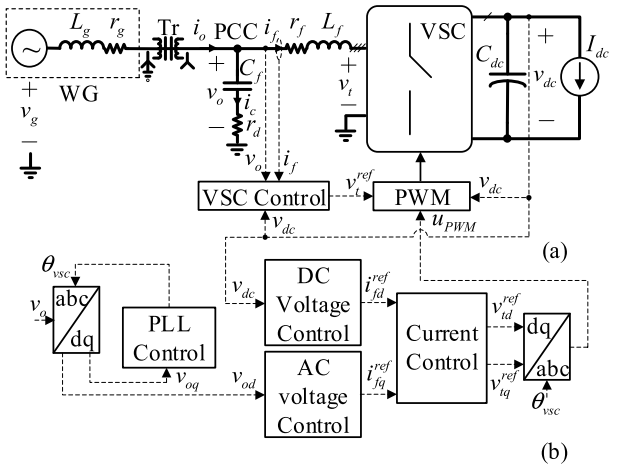

FIGURE 1. VSC-WG system. (a) VSC with *LC* filter connected to the utility grid through a step-down transformer and the grid impedance. (b) VSC control loops.

Section VI provides the large-signal simulation results. The real-time verification of the proposed method is presented in Section VII. Finally, the paper is concluded in Section VIII.

II. DYNAMIC MODEL OF THE VSC-WG SYSTEM

Fig. 1(a) shows a three-phase VSC in the rectification mode that is supplying a generic dc load at the dc-side with the nominal power P_n. The dc load is modeled by a current source in parallel with a dc filter capacitor. At the ac-side, the VSC, which is cascaded by an *LC* filter with a passive damping r_d [37], is connected to the PCC. The role of the *LC* filter in this arrangement is to reject the switching harmonics from affecting the VSC output voltage v_o. The PCC is connected to a step-down transformer Tr which, on the high-voltage side, is connected to a WG that is modeled as an ideal voltage source, with constant voltage v_g and constant frequency ω_g, i.e., infinite ac bus, in series with a high-value equivalent impedance. The WG impedance and Tr leakage impedance are lumped together and shown in Fig. 1(a) as an *RL* impedance with L_g and r_g as the inductive and resistive parts, respectively. The complete system parameters are depicted in Appendix A.

Fig. 1(b) shows the VOC control system which is established on the synchronous *dq*-RF. As shown, the PLL tracks the phase voltage angle at the PCC and generates the required frequency ω_{vsc} and the angle θ_{vsc} for the transformation of variables between stationary *abc*- and *dq*-RFs. The dynamic equations corresponding to the VSC-WG circuit and control loops, i.e., CC, PLL, DVC, and AVC, are presented in the following subsections. It should be noted that all equations are in the frequency domain and written in the *dq*-RF, wherein *s* represents the Laplace operator. To make the equations compact, they are presented in the matrix form and *dq* terms are labeled with subscript "$_{d,q}$" where necessary. Also, all the reference values and operating points are denoted by superscript "^{ref}" and "$^{\circ}$", respectively.

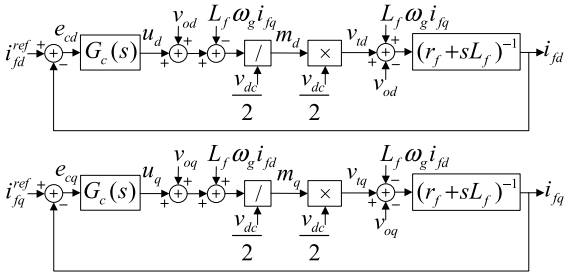

FIGURE 2. Block diagram of the CC loops.

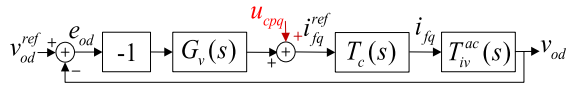

FIGURE 3. Block diagram of the AVC loop.

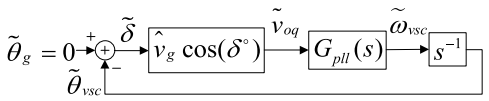

FIGURE 4. Block diagram of the PLL control loop.

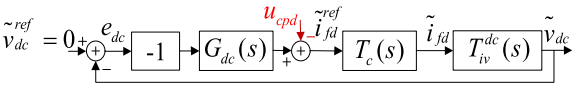

FIGURE 5. Block diagram of the DVC control loop.

A. POWER CIRCUIT DYNAMIC EQUATIONS

The circuit equations relating to the ac-side of the VSC-WG system in Fig. 1(a) are given in Appendix B for compactness.

B. CONTROL DYNAMIC EQUATIONS

The dynamic equations corresponding to the VSC-WG control system are developed in *dq*-RF and are presented in detail in Appendix B. Fig. 2 shows the block diagrams of the CC loops as the inner control loops that are identical in *dq* channels. The AVC is included in the VSC control system as the outer control loop to regulate the PCC voltage at the nominal value [5], [9], [20], [29]–[32]. Fig. 3 shows the control block diagram of the PCC voltage. Also, a compensating signal u_{cpq} is introduced to the forward loop in Fig. 3 which is discussed in Section V. The closed-loop diagram of the PLL used in this work is shown in Fig. 4. Fig. 5 shows the closed-loop block diagram of the DVC. As shown, a compensating signal denoted by u_{cpd} is added to the forward loop which will be discussed in Section V. The details about deriving the transfer functions used in Fig. 3−5 are also presented in Appendix B.

C. CONTROL DESIGN OF THE VSC-WG SYSTEM

The bandwidth (BW) of the CC loop is usually designed to remain in the range of 10−20% of the converter switching frequency [5]. The BWs of AVC and DVC loops are also considerably slower than the CC loop. The control objectives are to design the control loops in Figs. 2−5 with high BW and small overshoots (enough damping), while the closed-loop stability of the VSC-WG system is preserved at the nominal operating point. Consequently, the controller gains are obtained as presented in Appendix A. In summary, the BWs of {529, 29, 6} Hz are assigned to the CC, DVC, and AVC loops, respectively. Also, the BW of 26 Hz is assigned to the PLL loop to give reasonably fast-tracking dynamics to the PLL when subjected to fast changes in the operating point and at the same time filter the grid low-frequency harmonics [5], [39], [40].

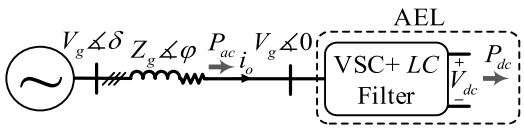

FIGURE 6. Active electronic load connected to the WG through an equivalent series impedance.

III. POWER-ANGLE LIMITATION AT LOW SCR

The VSC with the *LC* filter can be considered as an active electronic load (AEL) as seen by the WG. Fig. 6 shows a VSC with an *LC* filter in a compact form that interfaces the dc load to the ac grid. A series *RL* impedance $Z_g\angle\varphi$ is connecting the PCC bus and grid infinite bus with voltage phasors $V_g\angle 0$ and $V_o\angle\delta$, respectively. Since the PCC voltage is regulated at the nominal value V_g, the steady-state expression for the transferred real power P_{ac} according to Fig. 6 can be written as follows

$$P_{ac} = V_g^2 Z_g^{-1} \left(\cos(\varphi - \delta) - \cos(\varphi)\right) \tag{1}$$

which shows P_{ac} is a function of the phase angle difference δ.

According to the definition of *SCR* [18], the following can be written

$$SCR = V_g^2 (Z_g P_n)^{-1}. \tag{2}$$

Dividing both sides of (1) by P_n and using (2) give the per-unit value of the transferred power as follows

$$P_{ac}(pu) = SCR\left(\cos(\varphi - \delta) - \cos(\varphi)\right). \tag{3}$$

Assuming that the nominal power is transferred to the AL in Fig. 6, i.e., $P_{ac} = 1$ pu, the critical *SCR* (SCR^c) which is defined as the smallest *SCR* that the system can operate under the nominal condition according to the power-angle limit, is obtained at $\delta = \varphi$. Using the result in (3) gives the following

$$SCR^c = (1 - \cos(\varphi))^{-1} \tag{4}$$

which shows that SCR^c depends on the X/R ratio. Assuming a nonzero line resistance, X/R ratio is a finite value which results in φ less than $\pi/2$. Therefore, SCR^c for the VSC-WG system in the rectification mode is always more than unity according to (4). However, reversing the power to find the limit for *SCR* in the inversion mode, i.e., $P_{ac} = -1$ pu and $\delta < 0$, results in $SCR^c < 1$. Consequently, unlike the study

of the stability of the VSC-WG system in the inversion mode [38], the VWG condition in the rectification mode is at some SCR^c which is greater than unity assuming a WG condition.

IV. SMALL-SIGNAL STABILITY ASSESSMENT OF THE VSC-WG SYSTEM

The state-space model of the VSC-WG system without compensation signals, i.e., $u_{cpd,q} = 0$ in Figs. 3 and 5, is developed by linearizing the VSC-WG dynamic equations given in Appendix B at the nominal power level and using the parameters listed in Appendix A. The state-space model is represented in the matrix form as follows

$$\frac{d}{dt}\widetilde{\mathbf{X}}_{\mathbf{uc}} = \mathbf{A}_{\mathbf{uc}}\widetilde{\mathbf{X}}_{\mathbf{uc}} \tag{5}$$

where "~" signifies a small deviation in variables, $\mathbf{A_{uc}}$ is the state matrix as given in Appendix C, and $\widetilde{\mathbf{X}}_{\mathbf{uc}}$ is the state vector as given by

$$\widetilde{\mathbf{X}}_{\mathbf{uc}} = \begin{bmatrix} \widetilde{d} & \widetilde{v}^c_{od} & \widetilde{v}^c_{oq} & \widetilde{i}^c_{fd} & \widetilde{i}^c_{fq} & \widetilde{v}^c_{dc} & \widetilde{i}_{fd} & \widetilde{i}_{fq} & \widetilde{v}_{cd} & \widetilde{v}_{cq} & \widetilde{i}_{od} & \widetilde{i}_{oq} & \widetilde{v}_{dc} \end{bmatrix}^T. \tag{6}$$

A. MODAL ANALYSIS

The nominal values of different states are obtained by solving the algebraic equations of the VSC-WG system at the nominal power operating point and under $SCR = 1.18$ condition. The algebraic equations can be obtained by setting s in the VSC-WG dynamic equations to zero. Then, $\mathbf{A_{uc}}$ in (5) is evaluated using the parameter values provided in Appendix A. Table 1 summarizes the results where the relative participation of a state in an eigenvalue (mode) is evaluated using the participation factor (PF) measure [43].

As shown in Table 1, the system is highly unstable due to the presence of two unstable complex eigenvalues in the low-frequency and high-frequency ranges, λ_{2-3} and λ_{4-5}, respectively. The presence of these unstable eigenvalues shows that while the VSC control loops are designed to retain stable dynamics under the nominal condition, the VOC-based VSC and WG interconnection bears highly unstable dynamics. According to the PF analysis in Table 1, PLL, AVC, and DVC show strong participation in λ_{2-3} while λ_{4-5} is mostly affected by dc-side and ac network states. Moreover, ac network states have moderate participation in λ_{2-3}. Therefore, the dynamic interaction between the VSC control dynamics and the WG impedance is the primary source of instability in the VSC-WG system. There is also real stable eigenvalue λ_1 which corresponds to the PLL states and the WG states do not show any participation in it.

B. SENSITIVITY ANALYSIS

1) VSC POWER LEVEL

Fig. 7 demonstrates how the dominant eigenvalues relocate as the VSC active power P_{ac} changes from 0.82 to 1 pu. As shown in Fig. 7(a) for rectification mode, initially both dominant complex eigenvalues λ_{2-3} and λ_{4-5} are in the left half-plain (LHP). As P_{ac} increases, λ_{4-5} have significant

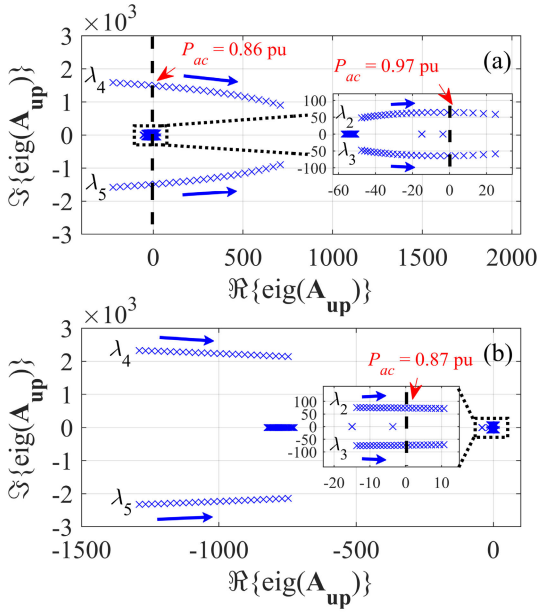

FIGURE 7. Spectrum of the dominant eigenvalues when P_{ac} changes between 0.82 to 1 pu in the (a) rectification mode and (b) inversion mode.

move towards the $j\omega$ axis while λ_{2-3} exhibit mild movement in the same direction. Therefore, the stability of the VSC-WG system diminishes as the active power increases. Moreover, the VSC-WG system is not stable at $P_{ac} = 0.86$ pu since λ_{4-5} enter right HP (RHP). Eventually, λ_{2-3} enters the RHP at $P_{ac} = 0.97$ pu as well. Therefore, the VSC-WG system is unstable under the nominal condition due to the movement of two separate pairs of complex eigenvalues into the RHP. Fig. 7(b) shows the relocation of the dominant eigenvalues as a result of the same changes in the power level in the inversion mode of operation. As shown, λ_{4-5} relocation is limited to the LHP, while λ_{2-3} cross the $j\omega$ axis and the system becomes unstable at $P_{ac} = 0.87$ pu. This shows that first, the stability of the VSC-WG system at the nominal ac power is mostly influenced by the dominant low-frequency (range) eigenvalues and high-frequency (range) eigenvalues in the rectification mode and the inversion mode, respectively; second, the stability of the system in the inversion mode is slightly better than the rectification mode.

2) PASSIVE DAMPING

The effect of adding a series damping resistance r_d to the VSC LC filter on the dominant eigenvalues of the VSC-WG system is shown in Fig. 8. According to the figure, λ_{4-5}, that are initially in the RHP, slightly relocate toward the $j\omega$ axis and then move in the opposite direction as a function of increasing r_d from zero. As shown, the system remains unstable at the nominal active power. Therefore, passive damping is not able to mitigate the VSC-WG instability problem. However, a value is assigned to r_d to damp the LC filter resonance peak during light-load conditions and without extra power loss under the VWG condition as given in Appendix A.

TABLE 1. Participation factor of the states in the dominant modes.

Subsystem	State	Dominant Eigenvalues of $\mathbf{A_{uc}}$ at P_{ac} = 1 pu and SCR = 1.18		
		$\lambda_1 = -4$	$\lambda_{2\text{-}3} = 20 \pm 60j$	$\lambda_{4\text{-}5} = 681 \pm 942j$
AC Network	$\tilde{i}_{od}$	~0	0.2	2.5
	$\tilde{i}_{oq}$	~0	0.3	1.1
	$\tilde{i}_{fd}$	~0	0.26	1.1
	$\tilde{i}_{fq}$	~0	0.2	0.6
	$\tilde{v}_{cd}$	~0	~0	0.1
	$\tilde{v}_{cq}$	~0	~0	~0
PLL	$\tilde{\delta}$	~0	0.8	0.2
	$\tilde{v}^c_{oq}$	1	~0	~0
DC-Side	$\tilde{v}_{dc}$	~0	0.4	3.7
DVC	$\tilde{v}^c_{dc}$	~0	0.5	0.2
AVC	$\tilde{v}^c_{od}$	~0	0.7	0.2

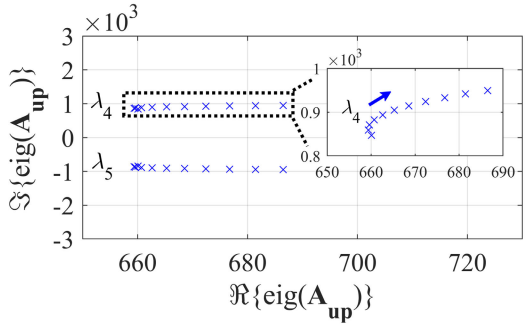

FIGURE 8. Spectrum of the dominant eigenvalues at $P_{ac} = 1$ pu when r_d changes between 0 to 1 Ω.

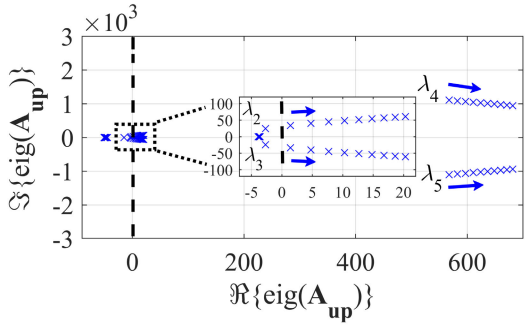

FIGURE 9. Spectrum of the dominant eigenvalues at $P_{ac} = 1$ pu when ($K_{p\omega}$,$K_{i\omega}$) change by a gain of 0.1 to 1.

3) PLL

The effect of changing the PLL bandwidth on the system stability is studied by changing the PLL gains ($K_{p\omega}$, $K_{i\omega}$) by a gain of 0.1 to 10. The effect of these changes on the relocation of the dominant eigenvalues is found under the nominal condition and is summarized in Fig. 9. As demonstrated, λ_{4-5} progress in the RHP in the unstable direction while, λ_{2-3}, which are initially in the LHP, move towards RHP. Fig. 9 shows that λ_{2-3} are less affected by the changes in the control gains as compared to λ_{2-3}. Moreover, by decreasing the PLL gains by 10 degrees of magnitude, which limits the PLL BW to 3 Hz, the VSC-WG system remains unstable at the nominal active power.

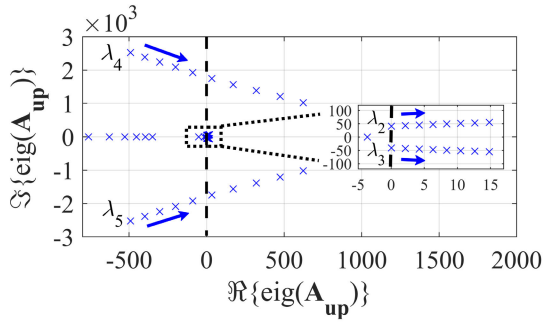

FIGURE 10. Spectrum of the dominant eigenvalues at $P_{ac} = 1$ pu when (K_{pdc},K_{idc}) change by a gain of 0.5 to 1.

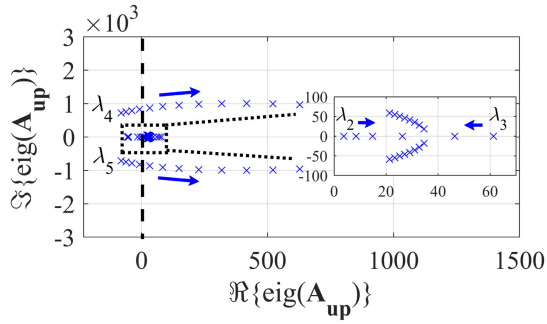

FIGURE 11. Spectrum of the dominant eigenvalues considering the active compensation at $P_{ac} = 1$ pu when (K_{pv},K_{iv}) change by a gain of 0.08 to 1.

4) DC VOLTAGE CONTROL

DVC gains are changed in this part to investigate their influence on the dominant eigenvalues of the VSC-WG system at the nominal power. Fig. 10 shows the progress of the eigenvalues towards the imaginary axis as the controller gains (K_{pdc}, K_{idc}) are changed by a gain of 0.5 to 1. As shown, the complex pair λ_{4-5}, that are initially in the LHP, approach the imaginary axis as a result of changes in the control gains until they cross the axis, where the BW of the DVC is 17 Hz. Further increase in the gains results in the relocation of the eigenvalues into the RHP. Meanwhile, λ_{2-3} move in the same direction as λ_{4-5} yet constantly in the RHP. This shows that the instability problem of the VSC-WG system exists within a wide range of variations in the BW of the DVC.

5) AC VOLTAGE CONTROL

The effect of varying the AVC gains on the dominant eigenvalues of the VSC-WG system at the nominal active power is depicted in Fig. 11. According to the figure, similar to changing DVC gains, λ_{4-5} are initially in the LHP. Then, by multiplying the control gains (K_{pv}, K_{iv}) by a gain of 0.08 to 1,

they progress extensively towards the unstable region and enter the RHP, where the BW of the AVC is 2.5 Hz. Meanwhile, λ_{2-3}, that initially have real form, relocate slightly until they merge and turn into a complex pair, still in the RHP, suggesting that the system remains unstable during the whole movement. Parallel to this relocation, the BW of the AVC increases from 0.5 to 5.5 Hz.

V. PROPOSED DUAL ACTIVE COMPENSATOR TO IMPROVE THE STABILITY OF THE VSC-WG IN THE RECTIFICATION MODE

The sensitivity analysis in Section III shows that the stability of the VSC-WG system is violated at the nominal active power due to the dynamic interaction between the VSC control system and the WG impedance. The instability can be avoided only under the condition that the DVC dynamics are extremely compromised which is not desired. To mitigate this issue, a DAC scheme is proposed by which, two linear functions of the VSC output voltage are added to the AVC and DVC loops to change the distribution of the system eigenvalues in the complex plane and stabilize the system at the nominal power without compromising the system dynamics. Moreover, the system damping is increased under lower levels of power.

As shown in Figs. 3 and 5 in red, the feed-forward compensators $u_{cpd,q}$ are added to the DVC and AVC closed-loop systems, respectively. Based on these augmentations, the equations for current references can be rewritten as

$$i_{fd}^{ref} = -G_{dc}(s)e_{dc} - u_{cpd}(s) \tag{7}$$

$$i_{fq}^{ref} = -G_{v}(s)e_{od} + u_{cpq}(s). \tag{8}$$

The compensators $u_{cpd,q}$ in (7) and (8) are linear transfer functions of the VSC output voltage terms $v_{od,q}$ as defined by the following

$$u_{cpd}(s) = K_{cpd}\frac{2\xi\omega_{cpd}s}{s^2 + 2\xi\omega_{cpd}s + \omega_{cpd}^2}v_{od} \tag{9}$$

$$u_{cpq}(s) = K_{cpq}\frac{\omega_{cpq}}{s + \omega_{cpq}}v_{oq} \tag{10}$$

where K_{cpd}, ξ, and ω_{cpd} are the gain, damping ratio, and center frequency of the band-pass filter (BPF) corresponding to u_{cpd}; and K_{cpq} and ω_{cpq} are the (dc) gain and cut-off frequency of the low-pass filter (LPF) corresponding to u_{cpq}. Based on the PFs of $\tilde{v}_{dc}$ and $\tilde{v}_{od}^{c}$ in the dominant eigenvalues of the VSC-WG system as given by Table 1, the BPF in (9) is selected to affect the unstable modes corresponding to eigenvalues λ_{4-5} in the high-frequency range without any undesired effect on other frequency ranges. Moreover, the LPF in (10) is selected to affect the unstable modes corresponding to the low-frequency range dominant eigenvalues λ_{2-3}. Since v_{od} is constant and v_{oq} is zero in the steady state, the compensators have zero effects on the steady-state operation of the VSC according to (9) and (10).

A. LINEAR MODEL OF THE COMPENSATED VSC-WG SYSTEM

The VSC-WG with the DAC is linearized in this part similar to the uncompensated model in Section IV using the same dynamic equations with the exception of considering nonzero compensation signals as given in (7) and (8). The linearized model of the compensated VSC-WG system is presented as follows

$$\frac{d}{dt}\widetilde{\mathbf{X}}_{\mathbf{cp}} = \mathbf{A}_{\mathbf{cp}}\widetilde{\mathbf{X}}_{\mathbf{cp}} \tag{11}$$

where the state matrix $\mathbf{A}_{\mathbf{cp}}$ is shown in Appendix C and the states vector $\widetilde{\mathbf{X}}_{\mathbf{cp}}$ is given as

$$\widetilde{\mathbf{X}}_{\mathbf{cp}} = \begin{bmatrix} \widetilde{\mathbf{X}}_{\mathbf{uc}}^{T} & x_{cpq} & x_{cpd1} & x_{cpd2} \end{bmatrix}^{T} \tag{12}$$

where x_{cpd1-2} and x_{cpq}, are the new state variables that are introduced by the BPF and LPF in (9) and (10).

B. DESIGN AND ANALYSIS OF DAC COMPENSATION

The DAC compensators presented in (9) and (10) are three and two degrees of freedom controllers, respectively. The root locus method is used to find the optimum values of the DAC parameters using the state-space model of the compensated VSC-WG system as given in (11). The effect of changing different DAC parameters on the dominant eigenvalues of the VSC-WG system is obtained at the nominal power under *SCR* = 1.18 condition. The summary of the results is shown in Fig. 12. Fig.12(a) shows the migration of λ_{4-5} as a function of the increase in the BPF gain K_{cpd} at $\omega_{cpd} = \{300, 600, 900\}$ rad/s while the u_{cpq} compensator is disabled by setting K_{cpq} to zero.

As shown, λ_{4-5}, that are initially located in the RHP, move towards the $j\omega$ axis as K_{cpd} increases. Moreover, the compensation effectiveness can be boosted by taking larger values of ω_{cpd}. As shown, at $\omega_{cpd} = \{600, 900\}$ rad/s, λ_{4-5} enter the stable region (LHP). According to Fig. 12(a), the optimum frequency at which u_{cpq} applies maximum damping to the overall system dynamics is $\omega_{cpd} = 600$ rad/s. According to the figure, the effect of increasing K_{cpd} on the system damping is twofold. On one hand, λ_{4-5} move in the direction of increasing the system stability, on the other hand, λ_{6-7} move in the opposite direction decreasing the system stability. Therefore, a trade-off is considered to find the optimum value for K_{cpd} where the resulting value is given in Appendix A. Moreover, increasing the damping ratio ξ has a mild positive effect on the system damping (not shown in Fig. 12). Unlike λ_{4-5}, the low-frequency range eigenvalues λ_{2-3} are not affected by u_{cpq} compensator and remain in the unstable region (RHP).

Fig.12(b) shows the migration of λ_{2-3} as a function of the increases in the u_{cpq} compensator gain K_{cpq} at $\omega_{cpq} = \{5, 10, 15\}$ rad/s while the u_{cpd} compensator is enabled with the optimum parameters ($\omega_{cpd} = 600$ Hz and $K_{cpd} = 3.5$). As shown, λ_{2-3}, that are initially in the RHP, relocate and move towards the imaginary axis and enter the stable region. According to Fig. 12(b), the maximum improvement in the

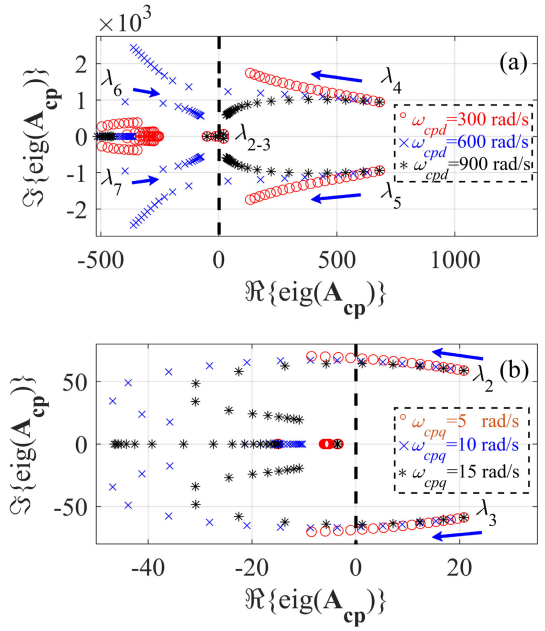

FIGURE 12. Spectrum of the dominant eigenvalues with DAC at $P_{ac} = 1$ pu and $SCR = 1.18$. (a) K_{cpd} varies from 0 to 5 and $K_{cpq} = 0$ at $\omega_{cpd} = (300, 600, 900)$ rad/s. (b) K_{cpq} varies from 0 to 400 at $\omega_{cpq} = (5, 10, 15)$ rad/s, $K_{cpd} = 3.5$, and $\omega_{cpd} = 600$ rad/s.

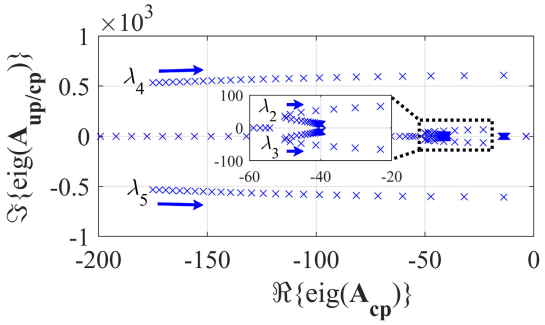

FIGURE 13. Spectrum of the dominant eigenvalues with DAC when P_{ac} changes from 0.85 pu to 1 pu.

system stability is reached at $\omega_{cpq} = 10$ rad/s and the optimum value of K_{cpd} is found at 225 where the dominant modes have the maximum damping. It should be noted that due to the frequency-scale separation between the BPF and LPF, the u_{cpd} and u_{cpq} dynamics are decoupled. Therefore, the DAC compensators $u_{cpd,q}$ can be designed independently. Moreover, the DAC can dynamically mitigate the unstable oscillations in both low-frequency and high-frequency ranges without any unwanted cross-coupling.

Fig. 13 shows the trajectory of the dominant eigenvalues of the VSC-WG system with the proposed DAC compensation subject to the increase of P_{ac} from 0.85 to 1 pu. As shown, λ_{4-5} progress towards the imaginary axis, similar to the uncompensated system in Fig. 7, nevertheless, constantly in the LHP. Moreover, λ_{2-3}, follow the same pattern as λ_{4-5} in the stable region but with a slower rate. Fig. 13, shows that the

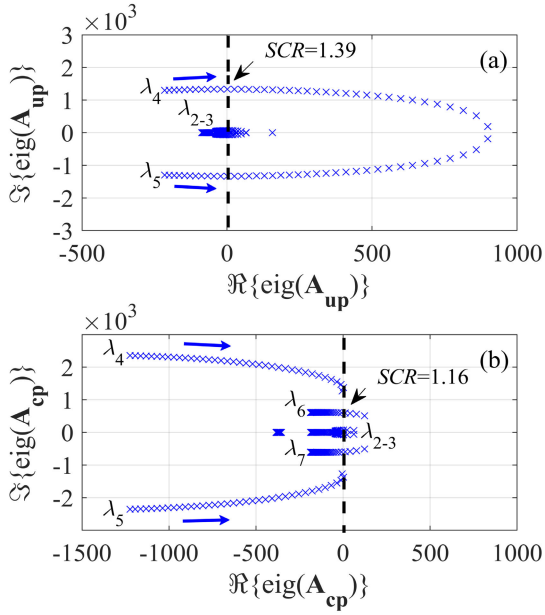

FIGURE 14. Spectrum of the dominant eigenvalues (a) without DAC. (b) with DAC when SCR changes from 1.5 to 1.1 ($= SCR^c$).

proposed DAC compensation improves the VSC-WG system stability for a wider range of active power (up to 1 pu) in the rectification mode as compared to the uncompensated system under the VWG condition.

Fig. 14 shows the progress of the dominant eigenvalues subject to changes in SCR from 1.5 to 1.1, which corresponds to the SCR^c level in (4) and the X/R ratio of 15. As shown in Fig. 14(a), λ_{4-5} move towards the imaginary axis and cross it at $SCR = 1.39$ as the SCR is decreased by increasing the grid impedance Z_g. According to Fig. 14(b), the dominant modes λ_{4-5} follow a similar trend but cross the imaginary axis at $SCR = 1.16$. Therefore, the DAC scheme extends the stability margin of the VSC-WG to a closer vicinity of the theoretical limit as compared to the uncompensated system.

VI. SIMULATION RESULTS

A series of time-domain simulations are carried out on the nonlinear model of the VSC-WG system to verify the results that are obtained based on the small-signal model that is developed in the previous sections. The VSC-WG shown in Fig. 1 is built in MATLAB/Simulink environment based on the system specifications that are provided in Appendix A. The average model of the VSC is used for the purpose of dynamic simulation [5].

A. RESPONSE TO ACTIVE POWER STEP-UP

The active power response of the VSC-WG system subject to the sequential power steps at different power levels is summarized in Fig. 15. A small step change is applied to the input of the VSC dc-side current source I_{dc} at $t = 0.1$ s at different power levels. As shown in Figs. 15(a)−(b), the responses of the VSC active power with and without DAC

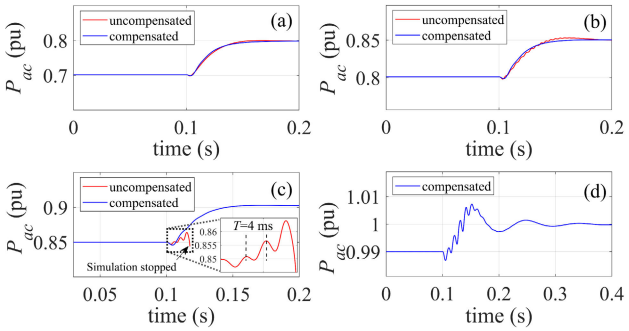

FIGURE 15. Dynamic response of the active power following a step variation in the active power at $t = 0.1$ s at different power levels in the rectification mode.

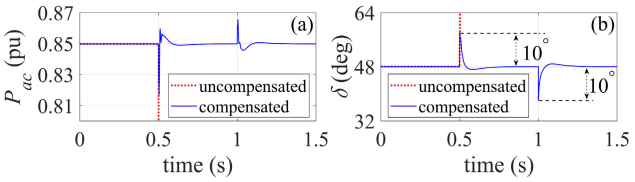

FIGURE 16. Transient responses of the VSC-WG with DAC scheme at $P_{ac} = 0.85$ pu during 10° step changes in the phase angle of the grid voltage. (a) active power response. (b) angle difference response.

are very close up to $P_{ac} = 0.85$ pu. At higher power levels, the responses begin to diverge. As shown in Fig. 15(c), the unstable oscillatory behavior is visible in the uncompensated system response P_{ac} is close to 0.85 pu while the response of the compensated system exhibits well-damped stable dynamics at the same power level. These oscillations relate to the relocation of λ_{4-5} to the RHP with the change in the power as observed in Fig. 7(a). Note that the period of the oscillations is 4 ms which closely matches the frequency of the corresponding eigenvalues λ_{4-5}, i.e., 1494 Hz, as they cross the imaginary axis in Fig. 7(a). More importantly, the VSC-WG system with enabled DAC demonstrates stable responses under the full range of the active power injection as shown in Figs. 15(a)−(d).

B. RESPONSE TO GRID ANGLE CHANGE

Another perk of using the proposed DAC scheme is the enhancement in the robustness of the VSC-WG system against the grid angle variations. Fig. 16 shows the VSC-WG responses where a 10-degree step disturbance happens in the grid voltage angle θ_g at the infinite ac bus at $t = 0.5$ s and is cleared in $t = 1$ s while the VSC-WG active power is $P_{ac} = 0.85$ pu. The power response of the compensated system is shown in Fig. 16(a) in blue. As shown, P_{ac} undergoes an undershoot and overshoot of about 0.03 and 0.01 pu at $t = 0.5$ and 1 s, respectively, yet the VSC controller manages to regulate the injected power at the nominal value. As shown in Fig. 16(b), there are overshoots and undershoots of 10 degrees in the VSC angle difference response δ following the changes in the grid angle. The VSC PLL tracks the actual PCC angle

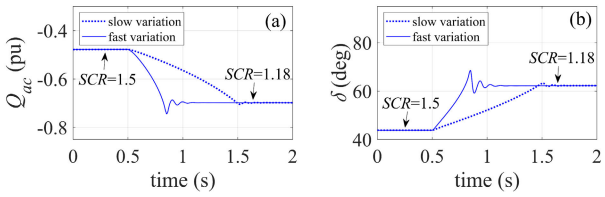

FIGURE 17. Transient responses of the VSC-WG with DAC scheme at $P_{ac} = 1$ pu when Z_g linearly increases at slow (0.33 s period) and fast rates (1s period). (a) reactive power response. (b) angle difference response.

and quickly updates the VSC angle. Since the VSC-WG active power is not changing, the value of δ returns to the same value right after changes. Moreover, the VSC-WG system stability is well preserved. The same condition is applied to the uncompensated VSC-WG system. As shown in Fig 16 with the dotted red line, the uncompensated system fails to track the deviations in the angle. Therefore, the VSC-WG does not reach a stable operating point.

C. RESPONSE TO GRID IMPEDANCE VARIATION

The grid equivalent impedance depends on the power flow especially in grid-connected microgrids where several DGs with plug-and-play capability are accommodated. Moreover, the disconnection of lines in the case of fault occurrence imposes a rapid change in the grid impedance. Therefore, the WG impedance is considered time-varying [9], [33], [41], [42].

Fig. 17 shows the responses of the VSC-WG system to the increase in the grid impedance Z_g. Since the rate of the change in the grid impedance is not *a priori* assumption, the simulation is repeated for two periods of 0.33 s and 1 s which represent fast and slow changes in the WG impedance, respectively. The system is initially in the steady-state stable condition at $SCR = 1.5$. Then, at $t = 0.5$ s, Z_g increases linearly from 0.8 pu to 1 pu and SCR decreases from 1.5 to 1 consequently while the VSC active power is at the nominal value. In the meantime, according to Fig. 17(a), Q_{ac} increases to compensate for the reactive power absorbed by the WG reactance and maintain the so-called voltage stability [42]. As shown in Fig. 17(b), δ increases as the grid reactance increases which is justified according to (1) knowing that the VSC-WG active power is not changing. There are overshoots and undershoots in the system responses during the fast-rate changes in the grid impedance. However, the stable operation of the system is maintained during both rates of change. According to Fig. 17, the stability of the VSC-WG system with DAC enabled is guaranteed under a wide range of fast and slow-rate changes in the grid impedance.

D. INTERACTION BETWEEN DAC AND VOC

The dynamic interactions of the proposed compensation method with the primary controllers of the VSC-WG control system are investigated at $P_{ac} = 0.85$ pu, where the system is naturally stable without the active compensation. Fig. 18(a) shows the frequency tracking responses of the PLL subject to

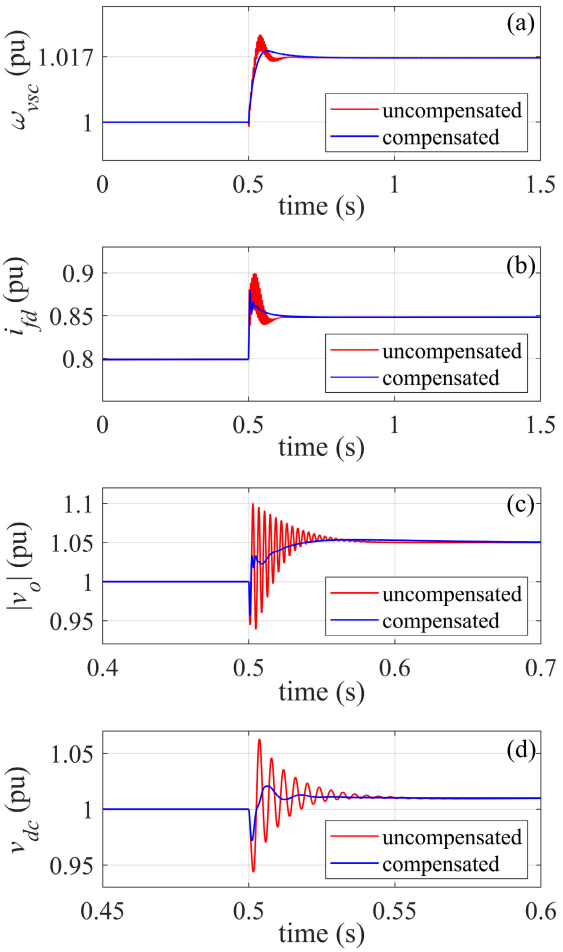

FIGURE 18. Dynamic responses of the VSC control loops subject to a step in the reference inputs at $t = 0.5$ s and $P_{ac} = 0.85$ pu. (a) frequency response following a 1 Hz grid frequency step. (b) d channel current response i_{fd} following a 5% in the current reference. (c) voltage response following a 5% step in the ac voltage reference. (d) dc voltage response following a 1% step in the dc voltage reference.

a 1 Hz step in the frequency of the grid at $t = 0.5$ s. Visibly, the DAC has an insignificant effect on the ω_{vsc} response and hence on the PLL dynamics. Fig. 18(b) shows the responses of i_{fd} following a 5% step in the current reference at $t = 0.5$ s. As shown, the proposed DAC scheme manages to substantially decrease the overshoots and suppress the oscillations. Fig 18(c) shows the variations in the magnitude of the PCC voltage $|v_o|$ following a 5% step change at $t = 0.5$ s. As shown, the proposed DAC scheme suppresses the oscillations in the uncompensated response without making the response sluggish. The variation of the dc voltage response v_{dc} is shown in Fig. 18(d). As shown, when the reference increases by 1% at $t = 0.5$ s, the compensated system exhibits a much more damped response with smaller over/undershoots as compared to the uncompensated system. Also, the system response speed is not compromised. Therefore, the outer control loop dynamics are not negatively affected by the introduction of the DAC feedforwards while benefiting from the compensators where the undesired oscillations are attenuated.

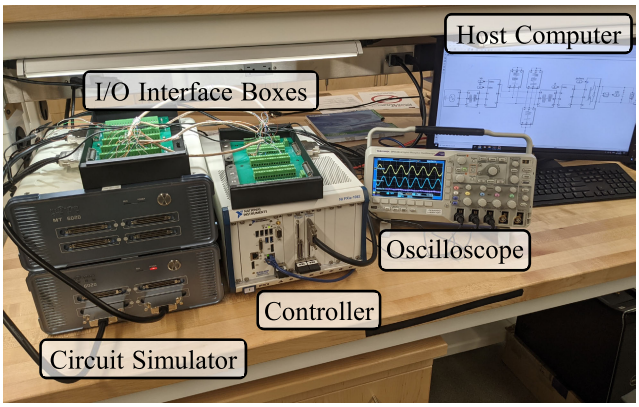

FIGURE 19. VSC-WG FPGA-based experimental set-up.

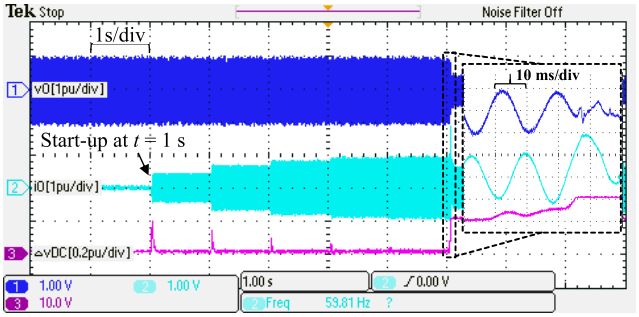

FIGURE 20. Measurement of the VSC-WG responses (DAC disabled) during start-up transients and step-ups in the dc power.

VII. HIL REAL-TIME VERIFICATION

To verify the simulation results about the effectiveness of the proposed DAC scheme in improving the VSC-WG stability in the rectification mode, the VSC-WG system in Fig. 1 is developed in the hardware-in-the-loop (HIL) system assuming the switched-model of the VSC as shown in Fig. 19. The HIL system essentially includes MT 6020 as an FPGA-based real-time circuit simulator and NI-PXIe-7868R CPU on which the VSC-WG controller is developed as shown in Fig. 19. Two I/O interface boxes are used to allow the physical connection between the circuit simulator and the controller. The emulated VSC-WG and the DAC parameter specifications follow the same values given in Appendix A. The time-step of the real-time simulation is 1 μs while the controller is running at 50 μs sampling time.

A series of tests are performed during which the VSC-WG active power is increased with a staircase profile $P_{ac} = [0.4, 0.6, 0.7, 0.75, 0.8, 0.88]$ with increases in the input of the current source I_{dc} at $t = [1, 2, 3, 4, 5, 6]$ s. Fig. 20 shows the responses of the VSC-WG system without DAC compensation. As shown in Fig. 20(a), v_o is regulated at 1 pu during the period $t = [0, 6)$ s due to the AVC action. As shown in Fig. 20, i_o increases after each step in the dc power and

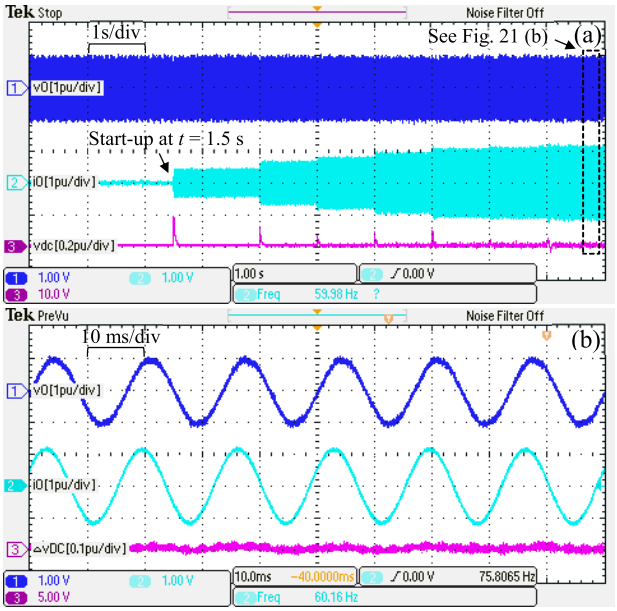

FIGURE 21. Measurement of the VSC-WG responses (DAC enabled) during start-up transients and step-ups in the dc current. (a) VSC output voltage/current (phase A) and dc-side voltage error. (b) zoomed view of the VSC responses in the steady state.

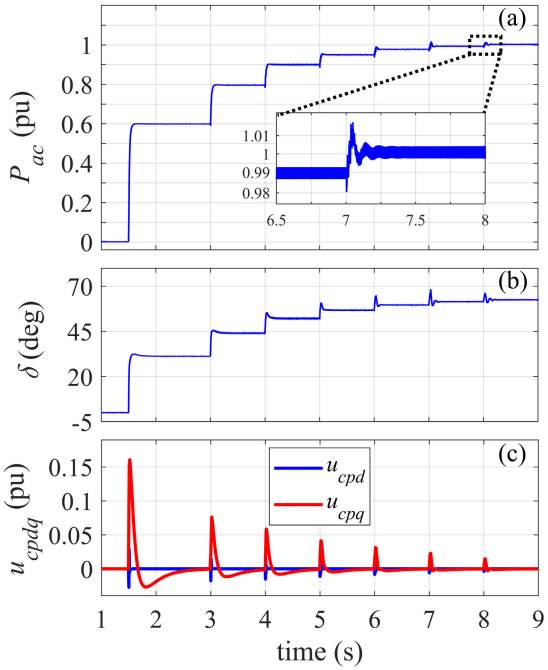

FIGURE 22. The VSC-WG responses (DAC enabled) during start-up transients and step-ups in the dc current (continued). (a) active power. (b) phase angle difference. (c) DAC compensation signals.

reaches a new steady-state point each time due to the CC action to maintain the power balance between the dc and ac-sides of the VSC. The difference of the dc-side voltage from the reference value (dc-side voltage error) Δv_{dc} is depicted in Fig. 20. According to Fig. 20, VSC-WG system operation is stable during the period $t = [0, 6)$ s. However, with further increases in the P_{ac} at $t = 6$ s, the Δv_{dc} response shows undamped oscillations as shown in the zoom window superimposed on Fig. 20. As shown, the VSC-WG system is unstable at $P_{ac} = 0.88$ pu which agrees with the small-signal result in Fig. 7(a) where λ_{4-5} are in the unstable region at the same power level. Moreover, the unstable oscillations are more pronounced in the Δv_{dc} response as compared to the other responses in Fig. 20 since v_{dc} has the largest participation in the eigenmode related to λ_{4-5} according to Table 1.

Similar series of tests are repeated for the VSC-WG system with DAC enabled. The active power profile is given as $P_{ac} = [0.6, 0.8, 0.9, 0.95, 0.97, 0.99, 1]$ pu with the increases in I_{dc} at $t = [1.5, 3, 4, 5, 6, 7, 8]$ s. Fig. 21(a) shows the experimental results. As shown, the system is stable and the v_o, i_o, and Δv_{dc} responses are well-damped and regulated in the steady state during the period $t = [0, 9]$ s. The undershoots in the Δv_{dc} response in Fig. 21(a) are less than 0.2 during the start-up and at the beginning of each step. Despite them, the VSC-WG system is stable at the nominal active power under the VWG condition.

Fig. 21(b) shows a closer view of the VSC-WG responses in the steady-state under the nominal condition where the switching ripple content is pronounced for ac and dc-side voltages. Due to the filtering effect of the WG large inductance, the VSC output current is almost ripple-free as shown in Fig. 21(b). It should be noted that the total harmonic distortion of v_o in Fig. 21(b) is smaller than 5% which complies with the IEEE standard 519 [44]. As shown in Fig. 21(b), the switching ripples are translated into the dc-side response Δv_{dc} as well. Yet, their content is negligible as compared to the average value of v_{dc} which is regulated at the nominal value by the DVC.

Fig. 22(a) shows the active power response P_{ac} of the VSC-WG system. The response is well-damped up to $P_{ac} = 0.95$ pu after which, small oscillations appear in the waveform. Regardless of the small oscillations in the waveform, the system is stable at the nominal power. Moreover, the dynamic response of P_{ac} around $t = 7$ s, as magnified by the zoom window in Fig. 22(a), and the response of the average model in Fig. 15(d) closely matches. This verifies the development of the small-signal model in Section V. Fig. 22(b) shows the angle difference response δ. Initially, δ is close to zero since the VSC active power is zero. By increasing P_{ac} and noting the output voltage is regulated at 1 pu, δ increases once the power increases according to (1). Fig. 22(c) shows the variations in the DAC signals $u_{cpd,q}$. As shown in Fig. 22(c), the compensation signals are activated during the transient conditions while they have zero impact on the system in the steady state. Moreover, due to the frequency separation of the LPF and BPF function, $u_{cpd,q}$ responses are visibly separable in terms of dynamic response.

VIII. CONCLUSION

Throughout this work, the integration of VSCs into the VWG systems has been investigated. The instabilities associated with the dynamic interaction between the VOC-based VSC in the rectification mode and the grid impedance have been

mitigated effectively using the proposed DAC scheme under the VWG condition. The DAC scheme includes the injection of modified versions of the PCC voltage into the dq current references of the CC loops. It is shown that the proposed DAC scheme contributes successfully to the relocation of the eigenvalues on the complex plane from the unstable region to more damped locations in the stable region. In addition to the stabilization of the VSC-WG system under the VWG conditions, the stability/robustness of the system subject to the grid angle deviations has been improved with the proposed DAC. The effectiveness of the proposed DAC has been validated analytically using the small-signal analysis and numerically using the large-signal nonlinear model of the VSC-WG system which is developed in MATLAB/SIMULINK and then tested in real time using a HIL experimental set-up. The proposed DAC has the following features: (1) it is simple and can be easily designed using the linear control tools, (2) it does not impact the steady-state condition of the VSC-WG system, (3) it has a minimal influence on the existing VOC system of the VSC and so it can be designed independently, (4) it requires no extra sensors for practical implementation. Time-domain simulations and experiments of the VSC-WG system are carried out to verify (1), the stability of the VSC-WG system with the proposed DAC scheme under VWG condition, (2) the improved damping property of the compensated VSC-WG system, (3) the enhanced capability of the VSC-WG system to withstand sudden grid angle deviations and wide range of variations in the grid impedance.

APPENDIX A

Parameters of the VSC-WG system are provided in Table 2.

TABLE 2. Parameters of VSC-WG system.

Parameter	Value	Unit
Nominal line-to-line rms voltage, V_g	13.8	kV
VSC rated dc power, P_n	7.25	MW
Nominal frequency, ω_g	377	rads^{-1}
Grid inductance, L_g	58.92	mH
Grid resistance, r_g	1.48	Ω
Transformer voltage ratio, a	13.8/0.6	kV/kV
Filter inductance, L_f	100	μH
Filter resistance, r_f	1.5	mΩ
PCC filter capacitance, C_f	500	μF
Filter resistance, r_d	0.9	Ω
DC-Side filter capacitance, C_{dc}	15	mF
DC-Side nominal voltage, V_{dc}	1.9	kV
PLL control gains, K_{po}, K_{io}	0.7, 2.5	rads^{-1}V^{-1}, rads^{-2}V^{-1}
CC gains, K_{pc}, K_{ic}	0.34, 5	Ω, Ωs^{-1}
AVC gains, K_{pv}, K_{iv}	5, 1000	Ω^{-1}, Ω^{-1}s^{-1}
DVC gains, K_{pdc}, K_{idc}	9, 450	Ω^{-1}, Ω^{-1}s^{-1}
Active compensator gains, K_{cpd}, K_{cpq}	3.5, 225	Ω^{-1}
Active compensator frequencies, ω_{cpd}, ω_{cpq}	600, 10	rads^{-1}
VSC switching frequency, f_s	3040	Hz
ON-state resistance of VSC switches, r_{on}	0.88	mΩ
Forward voltage drop of VSC switches, V_f	1	V

APPENDIX B

A. POWER CIRCUIT EQUATIONS

Based on Fig. 1(a), the VSC-WG circuit equations at the ac- side are described by (A1)−(A4) where v_c is the voltage across the ac-side filter capacitor C_f, $Z_f(s) = r_f + s\omega_g L_f$, and $Z_g(s) = r_g + s\omega_g L_g$

$$\begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} = \begin{bmatrix} v_{od} \\ v_{oq} \end{bmatrix} + Z_f(s) \begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} + \omega_{vsc} L_f \begin{bmatrix} -i_{fq} \\ i_{fd} \end{bmatrix} \quad \text{(A1)}$$

$$\begin{bmatrix} v_{od} \\ v_{oq} \end{bmatrix} = \begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} + Z_g(s) \begin{bmatrix} i_{od} \\ i_{oq} \end{bmatrix} + \omega_{vsc} L_g \begin{bmatrix} -i_{oq} \\ i_{od} \end{bmatrix} \quad \text{(A2)}$$

$$\begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} = \begin{bmatrix} i_{od} \\ i_{oq} \end{bmatrix} + sC_f \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} + \omega_{vsc} C_f \begin{bmatrix} -v_{cq} \\ v_{cd} \end{bmatrix} \quad \text{(A3)}$$

$$\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} = \begin{bmatrix} v_{od} \\ v_{oq} \end{bmatrix} - r_d \begin{bmatrix} i_{fd} - i_{od} \\ i_{fq} - i_{oq} \end{bmatrix}. \quad \text{(A4)}$$

B. CURRENT CONTROL

A pair of similar proportional-and-integral (PI) compensators $G_s(s) = K_{pc} + K_{ic}s^{-1}$, regulates $i_{fd,q}$ to follow the reference values $i_{fd,q}^{ref}$. The voltage feedforwards and decoupling current terms are introduced to the forward paths in Fig. 2 to decouple the dq CC dynamics and cancel the effect of disturbance inputs $v_{od,q}$ when plugged into (A1) [5]. The expressions for the control inputs $u_{d,q}$ according to Fig. 2 are given by

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = G_c(s) \begin{bmatrix} i_{fd}^{ref} - i_{fd} \\ i_{fq}^{ref} - i_{fq} \end{bmatrix}. \quad \text{(A5)}$$

As shown in Fig. 2, the modulation indices $m_{d,q}$ are defined as

$$\begin{bmatrix} m_d \\ m_q \end{bmatrix} = \left(\begin{bmatrix} u_d \\ u_q \end{bmatrix} + \omega_{vsc} L_f \begin{bmatrix} -i_{fq} \\ i_{fd} \end{bmatrix} + \begin{bmatrix} v_{od} \\ v_{oq} \end{bmatrix} \right) \frac{2}{v_{dc}^{ref}}. \quad \text{(A6)}$$

If the PWM dynamics are neglected and the VSC averaged model [5] is considered, the VSC terminal voltages can be obtained from the following

$$\begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} = \begin{bmatrix} m_d \\ m_q \end{bmatrix} \frac{v_{dc}^{ref}}{2}. \quad \text{(A7)}$$

Applying (A5)–(A7) into (A1) gives the CC closed-loop transfer function as

$$T_c(s) = \frac{K_{pc}s + K_{ic}}{L_f s^2 + (r_f + K_{pc})s + K_{ic}}. \quad \text{(A8)}$$

C. AC VOLTAGE CONTROL

According to Fig. 3, a PI compensator $G_v(s) = K_{pv} + K_{iv}s^{-1}$ is employed to regulate v_{od} to the reference value by processing the error signal $e_{od} = v_{od}^{ref} - v_{od}$; and u_{cpq} is the compensating signal. $G_v(s)$ issues the reference value i_{fq}^{ref} according to the following

$$i_{fq}^{ref} = -G_v(s)e_{od}. \quad \text{(A9)}$$

The ac transfer function from i_{fq} to v_{od}, denoted by $T_{iv}^{ac}(s)$, can be obtained by linearizing the expression for v_{od} in (A1)–(A2). Ignoring the transient excursions in the terms

related to ω_{vsc} [5] and assuming $i_{od,q} \approx i_{fd,q}$ [38], the following can be derived by perturbing (A2)

$$\widetilde{v}_{od} = Z_g(s)\widetilde{i}_{od} - L_g\omega^{\circ}_{vsc}\widetilde{i}_{oq}. \tag{A10}$$

In (A10), $\widetilde{i}_{od}$ is the disturbance input. Thus, $T^{ac}_{iv}(s)$ may be obtained as

$$T^{ac}_{iv}(s) = -L_g\omega^{\circ}_{vsc}. \tag{A11}$$

As shown in Fig. 3, a negative gain is added to the forward path to cancel the negative sign of $T^{ac}_{iv}(s)$ in (A11). A more accurate treatment for obtaining the ac transfer function without ignoring the frequency deviations is presented in [38].

D. DQ-FRAME SYNCHRONISATION

As shown in Fig. 4, a conventional PLL system is used to track the angle of the PCC phase voltage. This is done by employing a PI controller $G_{pll}(s) = K_{p\omega} + K_{i\omega}s^{-1}$ that regulates the q component of the voltage v_{oq} to zero. Therefore, the following can be derived for the PLL dynamics

$$\omega_{vsc} = G_{pll}(s)v_{oq} \tag{A12}$$

$$\delta = \theta_g - \theta_{vsc} = (\omega_g - \omega_{vsc})s^{-1} \tag{A13}$$

where ω_{vsc} and θ_{vsc} are, the VSC frequency and phase angle generated by the PLL, respectively; ω_g and θ_g are the frequency and the phase angle of the grid voltage source, respectively; and $\delta = \theta_g - \theta_{vsc}$ is the phase angle difference.

E. DC VOLTAGE CONTROL

The dc-side voltage error $e_{dc} = {v_{dc}}^{ref} - v_{dc}$ passes through a PI compensator $G_{dc}(s) = K_{pdc} + K_{idc}s^{-1}$ and the result is used as a reference for the d channel of the CC. Therefore, the following relation between e_{dc} and ${i_{fd}}^{ref}$ exists

$${i_{fd}}^{ref} = G_{dc}(s)e_{dc}. \tag{A14}$$

The VSC dc-side power P_{dc} is equal to the sum of the instantaneous active power at the VSC terminals and in the dc filter capacitor C_{dc} neglecting the switching loss in the VSC. The dc transfer function from i_{fd} to v_{dc}, denoted by ${T_{iv}}^{dc}(s)$, is obtained as follows. First, the following expression is derived based on instantaneous power equilibrium [5]

$$\begin{aligned} v_{dc}I_{dc} = {} & 1.5(v_{od}i_{fd} + v_{oq}i_{fq}) - 0.75L_f s({i_{fd}}^2 + {i_{fq}}^2) \\ & -1.5r_f({i_{fd}}^2 + {i_{fq}}^2) - 0.5C_{dc}s{v_{dc}}^2. \end{aligned} \tag{A15}$$

Second, since (A15) is nonlinear with respect to v_{dc}, it is linearized at the nominal operating point. The result is given as follows where ${v_{oq}}^{\circ}$ is set to zero due to the PLL action

$$\begin{aligned} & (C_{dc}v^{\circ}_{dc}s + I_{dc})\widetilde{v}_{dc} \\ & = 1.5(v^{\circ}_{od}\widetilde{i}_{fd} + i^{\circ}_{fd}\widetilde{v}_{od} + i^{\circ}_{fq}\widetilde{v}_{oq}) - 1.5L_f s(i^{\circ}_{fd}\widetilde{i}_{fd} \\ & \quad + i^{\circ}_{fq}\widetilde{i}_{fq}) - 3r_f(i^{\circ}_{fd}\widetilde{i}_{fd} + i^{\circ}_{fq}\widetilde{i}_{fq}). \end{aligned} \tag{A16}$$

Rearranging (A16) to isolate $\widetilde{v}_{dc}$ and considering $\widetilde{i}_{fq}$ and $\widetilde{v}_{od,q}$ as the disturbance inputs result in the dc transfer function as follows

$$T^{dc}_{iv}(s) = -\frac{3}{2}\frac{L_f i^{\circ}_{fd}s + 2r_f i^{\circ}_{fd} - v^{\circ}_{od}}{C_{dc}v^{\circ}_{dc}s + I_{dc}}. \tag{A17}$$

Fig. 5 shows the DVC closed-loop diagram where a negative gain is considered in the forward path to cancel the negative sign of ${T_{iv}}^{dc}(s)$.

APPENDIX C

The state matrices introduced in the main body of the paper are provided in detail. $\mathbf{A_{up}} = \mathbf{A_{cp}}(i,j)$ for $1 \le i, j \le 13$ and $\mathbf{A_{cp}}$ is shown at the bottom of the next page. The corresponding parameters are $\Lambda_1 = i^{\circ}_{fd} + K_{pc}K_{pv}i^{\circ}_{fq}$, $\Lambda_2 = -v^{\circ}_{td} + (K_{pc} - r_d)\,i^{\circ}_{fd} - (L_f\omega_g + K_{pc}K_{pv}r_d)i^{\circ}_{fq}$, $\Lambda_3 = -v^{\circ}_{tq} + (K_{pc} - r_d)i^{\circ}_{fq} + L_f\omega_g i^{\circ}_{fd}$, $\Lambda_4 = K_{p\omega}r_d i^{\circ}_{od} - (r_d + r_g)L_g^{-1}$, $\Lambda_5 = K_{pc}K_{pc}r_d L_f^{-1} + \omega_g - \omega^{\circ}_{vsc}$, $\Lambda_6 = \omega^{\circ}_{vsc} - \omega_g + K_{p\omega}r_d i^{\circ}_{fq}$, $\Lambda_7 = -(r_f + K_{pc})L_f^{-1} - K_{p\omega}r_d i^{\circ}_{fd}$, $\Lambda_8 = (2/3)i^{\circ}_{dc} - K_{pc}K_{pdc}i^{\circ}_{fd}$, $\Lambda_9 = \omega^{\circ}_{vsc} - K_{p\omega}r_d i^{\circ}_{oq}$, $\Lambda_{10} = K_{p\omega}r_d v^{\circ}_{cd} - C_f^{-1}$, $\Lambda_{11} =$

$$\mathbf{A_{cp}} = \begin{bmatrix}
0 & 0 & -K_{i\omega} & 0 & 0 & 0 & 0 & K_{p\omega}r_d & 0 & -K_{p\omega}r_d & 0 & -K_{p\omega} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & r_d & 0 & -r_d & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -r_d & 0 & r_d & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -K_{idc} & 0 & 0 & -1 & 0 & 0 & 0 & K_{pdc} & 0 & -1 & 0 \\
0 & -K_{iv} & 0 & 0 & 0 & 0 & -K_{pv}r_d & 0 & K_{pv}r_d & -1 & K_{pv} & 0 & 0 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\
\frac{v^{\circ}_{gq}}{L_g} & 0 & K_{i\omega}i^{\circ}_{oq} & 0 & 0 & 0 & \frac{r_d+r_g}{-L_g} & \Lambda_9 & \frac{r_d}{L_g} & K_{p\omega}r_d i^{\circ}_{oq} & \frac{1}{L_g} & K_{p\omega}i^{\circ}_{oq} & 0 & 0 & 0 & 0 \\
\frac{v^{\circ}_{gd}}{-L_g} & 0 & -K_{i\omega}i^{\circ}_{od} & 0 & 0 & 0 & -\omega^{\circ}_{vsc} & \Lambda_4 & 0 & \Lambda_{11} & 0 & \Lambda_{12} & 0 & 0 & 0 & 0 \\
0 & 0 & K_{i\omega}i^{\circ}_{fq} & \frac{K_{ic}}{L_f} & 0 & \frac{K_{pc}K_{idc}}{-L_f} & 0 & -K_{p\omega}r_d i^{\circ}_{fq} & \frac{K_{pc}+r_f}{-L_f} & \Lambda_6 & 0 & K_{p\omega}i^{\circ}_{fq} & \frac{K_{pc}K_{pdc}}{L_f} & 0 & \frac{K_{pc}}{-L_f} & 0 \\
0 & \frac{K_{iv}K_{pc}}{-L_f} & -K_{i\omega}i^{\circ}_{fd} & 0 & \frac{K_{ic}}{L_f} & 0 & \frac{K_{pc}K_{pv}r_d}{-L_f} & K_{p\omega}r_d i^{\circ}_{fd} & \Lambda_5 & \Lambda_7 & \frac{K_{pc}K_{pv}}{L_f} & -K_{p\omega}i^{\circ}_{fd} & 0 & \frac{K_{pc}}{-L_f} & 0 & 0 \\
0 & 0 & K_{i\omega}v^{\circ}_{cq} & 0 & 0 & 0 & -C_f^{-1} & -K_{p\omega}r_d v^{\circ}_{cq} & C_f^{-1} & K_{p\omega}r_d v^{\circ}_{cq} & 0 & \Lambda_{13} & 0 & 0 & 0 & 0 \\
0 & 0 & -K_{i\omega}v^{\circ}_{cd} & 0 & 0 & 0 & 0 & \Lambda_{10} & 0 & -\Lambda_{10} & -\omega^{\circ}_{vsc} & -K_{p\omega}v^{\circ}_{cd} & 0 & 0 & 0 & 0 \\
0 & \sigma K_{pc}K_{iv}i^{\circ}_{fq} & 0 & -\sigma K_{ic}i^{\circ}_{fd} & -\sigma K_{ic}i^{\circ}_{fq} & \sigma K_{pc}K_{idc}i^{\circ}_{fd} & \sigma r_d\Lambda_1 & \sigma r_d i^{\circ}_{fq} & \sigma\Lambda_2 & \sigma\Lambda_3 & -\sigma\Lambda_1 & -\sigma i^{\circ}_{fq} & \sigma\Lambda_8 & \sigma K_{pc}i^{\circ}_{fq} & \sigma K_{pc}i^{\circ}_{fd} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -r_d K_{cpq}\omega_{cpq} & 0 & r_d K_{cpq}\omega_{cpq} & 0 & K_{cpq}\omega_{cpq} & 0 & -\omega_{cpq} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
\Lambda_{14} & 0 & \Lambda_{15} & \Lambda_{16} & 0 & \Lambda_{17} & \Lambda_{18} & \Lambda_{19} & \Lambda_{20} & \Lambda_{21} & \Lambda_{22} & \Lambda_{23} & \Lambda_{24} & 0 & \Lambda_{25} & -2\omega_{cpd}\xi
\end{bmatrix} \tag{A18}$$

$r_d(L_g^{-1} - K_{p\omega} i_{od}^{o})$, $\Lambda_{12} = L_g^{-1} - K_{p\omega} i_{od}^{o}$, $\Lambda_{13} = \omega_{vsc}^{o} + K_{p\omega} v_{cq}^{o}$, $\sigma = {}^{3}/_{2}(C_{dc} v_{dc}^{o})^{-1}$, $\rho = 2K_{cpd} r_d \omega_{cpd} \xi$, $\Lambda_{14} = -\rho V_g \sin(\delta_0) L_f^{-1}$, $\Lambda_{15} = \rho K_{i\omega}(v_{cq}^{o} r_d^{-1} + i_{fq}^{o} - i_{oq}^{o})$, $\Lambda_{16} = \rho K_{ic} L_f^{-1}$, $\Lambda_{17} = -\rho K_{idc} K_{pc} L_f^{-1}$, $\Lambda_{18} = -\rho(r_d^{-1} C_f^{-1} - (r_d + r_g)$, $\Lambda_{19} = -\rho(\omega_{vsc}^{o} + K_{p\omega} r_d i_{fq}^{o} L_g^{-1} + K_{p\omega} v_{cq}^{o} - K_{p\omega} r_d i_{oq}^{o})$, $\Lambda_{20} = \rho(r_d^{-1} C_f^{-1} - (K_{pc} + r_f) L_f^{-1} + L_g^{-1})$, $\Lambda_{21} = \rho(\omega_{vsc}^{o} - \omega_g + K_{p\omega} r_d i_{fq}^{o} + K_{p\omega} v_{cq}^{o} - K_{p\omega} r_d i_{oq}^{o})$, $\Lambda_{22} = -\rho L_g^{-1}$, $\Lambda_{23} = \rho((\omega_{vsc}^{o} + K_{p\omega} v_{cq}^{o}) r_d^{-1} + K_{p\omega} i_{fq}^{o} - K_{p\omega} i_{oq}^{o})$, $\Lambda_{24} = \rho K_{pdc} K_{pc} L_f^{-1}$, $\Lambda_{25} = -\omega_{cpd}^{2} - \rho K_{pdc} K_{pc} L_f^{-1}$.

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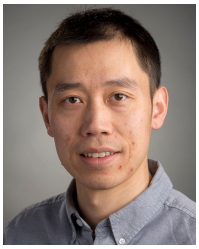

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